IN THE CLAIMS:

1. (Currently Amended) An emulating interface arrangement for a processor evaluation board and a DSP evaluation board, the processor evaluation board having a connector corresponding to actual data lines, address lines and control lines of a processor emulated by the processor evaluation board, the DSP evaluation board having a connector corresponding to actual data lines, address lines and control lines of a DSP emulated by the DSP evaluation board, the arrangement comprising:

a bridge board;

a processor connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the processor evaluation board;

a Digital Signal Processor (DSP) connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the DSP evaluation board;

a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection;

software included in said PLD for reading said address lines, said data lines and said control lines of said processor connection and said DSP connection, said software monitoring said lines and converting signals from said address lines, data lines and control lines of said processor connection into DSP transfer signals based on signals received from said DSP connection, said software transmitting said DSP transfer signals to said DSP connection, said software converting signals from said address lines, said data lines and said control lines of said

DSP connection into processor transfer signals based on signals received from said processor connection, said software transmitting said processor transfer signals to said processor connection, wherein said bridge board with said PLD and said software emulate a physical and electrical connection between a processor and a DSP in an Application Specific Integrated Circuit (ASIC).

2. (Canceled)

3. (Previously Presented) An emulating interface arrangement in accordance with claim 1, wherein:

one of said processor connection and said DSP connection is connectable to a power line of a respective processor evaluation board and a DSP evaluation board;

said PLD is powered from said one connection being connected to the power line.

4. (Previously Presented) An emulating interface arrangement in accordance with claim 1, wherein:

said processor connection is formed for connecting to a Spectrum Digital Incorporated TMS470 evaluation board;

said DSP connection is formed for connecting to a Spectrum Digital Incorporated TMS320LC54X evaluation board.

5. (Previously Presented) An emulating interface arrangement in accordance with claim 4, wherein:

said processor connection has structure to connect to JP1 and JP2 connectors of the Spectrum Digital Incorporated TMS470 evaluation board.

6. (Previously Presented) An emulating interface arrangement in accordance with claim 1, wherein:

said DSP connection includes a header to connect to conductive paths of the DSP evaluation board.

7. (Previously Presented) An emulating interface arrangement in accordance with claim 6, wherein:

said header is connectable to said conductive paths that correspond to a Host Port Interface (HPI) of the DSP evaluation board.

8. (Currently Amended) An emulating interface arrangement for a processor evaluation board and a DSP evaluation board, the processor evaluation board having a connector corresponding to actual data lines, address lines and control lines of a processor emulated by the processor evaluation board, the DSP evaluation board having a connector corresponding to actual data lines, address lines and control lines of a DSP emulated by the DSP evaluation board, the arrangement comprising:

a bridge board;

a processor connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the processor evaluation board;

a Digital Signal Processor (DSP) connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the DSP evaluation board;

a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection;

software included in said PLD for reading said address lines, said data lines and said control lines of said processor connection and said DSP connection, said software monitoring said lines and converting signals from said address lines, data lines and control lines of said processor connection into DSP transfer signals based on signals received from said DSP connection, said software transmitting said DSP transfer signals to said DSP connection, said software converting signals from said address lines, said data lines and said control lines of said DSP connection into processor transfer signals based on signals received from said processor connection, said software transmitting said processor transfer signals to said processor connection, wherein: said control lines include an interrupt line, a wait line, and a clock line.

9. (Currently Amended) An emulating interface arrangement for a processor evaluation board and a DSP evaluation board, the processor evaluation board having a connector corresponding to actual data lines, address lines and control lines of a processor emulated by

the processor evaluation board, the DSP evaluation board having a connector corresponding to actual data lines, address lines and control lines of a DSP emulated by the DSP evaluation board, the arrangement comprising:

a bridge board;

a processor connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the processor evaluation board;

a Digital Signal Processor (DSP) connection extending from said bridge board for connecting to ~~address lines, data lines and control lines of a~~ the connector of the DSP evaluation board;

a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection;

software included in said PLD for reading said address lines, said data lines and said control lines of said processor connection and said DSP connection, said software monitoring said lines and converting signals from said address lines, data lines and control lines of said processor connection into DSP transfer signals based on signals received from said DSP connection, said software transmitting said DSP transfer signals to said DSP connection, said software converting signals from said address lines, said data lines and said control lines of said DSP connection into processor transfer signals based on signals received from said processor connection, said software transmitting said processor transfer signals to said processor connection;

a processor evaluation board connected to said processor connection, said processor

evaluation board emulating the operation of a processor;

a DSP evaluation board connected to said DSP connection, said DSP evaluation board emulating the operation of a DSP.

10. (Previously Presented) An emulating interface arrangement in accordance with claim 9, further comprising:

a workstation connected to one of said processor evaluation board and said DSP evaluation board for configuring both of said processor evaluation board and said DSP evaluation board.

11. (Previously Presented) An emulating interface arrangement in accordance with claim 9, wherein:

said processor evaluation board and said DSP evaluation board include JTAG connectors for connecting to workstations which configure said processor evaluation board and said DSP evaluation board.

12. (Previously Presented) An emulating interface arrangement in accordance with claim 9, wherein:

said processor evaluation board, said bridge board and said DSP evaluation board emulate an ASIC with a processor connected to a DSP.

13. (Previously Presented) An emulating interface arrangement in accordance with claim 9, further comprising:

a power contact in one of said processor connection and said DSP connection for powering said bridge board with power from a respective one of said processor evaluation board and said DSP evaluation board.

14. (Previously Presented) An emulating interface arrangement in accordance with claim 9, wherein:

said processor emulation board is a Spectrum Digital Incorporated TMS470 evaluation board;

said DSP emulation board is a Spectrum Digital Incorporated TMS320LC54X evaluation board.

15. (Previously Presented) An emulating interface arrangement in accordance with claim 14, wherein:

said processor connection has structure to connect to JP1 and JP2 connectors of said Spectrum Digital Incorporated TMS470 evaluation board.

16. (Previously Presented) An emulating interface arrangement in accordance with claim 14, wherein:

said DSP connection includes a header to connect to conductive paths of said Spectrum

Digital Incorporated TMS320LC54X evaluation board.

17. (Previously Presented) An emulating interface arrangement in accordance with claim 16, wherein:

said header is connectable to said conductive paths that correspond to a Host Port Interface (HPI) of the DSP evaluation board.

18. (Currently Amended) An ASIC software emulator arrangement comprising:

a TMS320 evaluation board with signal lines corresponding to actual signal lines of TMS320 processor, said TMS320 evaluation board transferring data through said signal lines in a DSP format;

a TMS470 evaluation board with ~~processor signals~~ signal lines corresponding to actual signal lines of TMS470 processor, said TMS470 evaluation board transferring data in a processor format;

a bridge board connected to said signal lines of said TMS470 evaluation board and said TMS320 evaluation board, said bridge board converting data in said processor format on said TMS470 evaluation board into DSP format and onto said TMS320 evaluation board, said ~~translation~~ bridge board also converting data in said DSP format on said TMS320 evaluation board into said processor format and onto said TMS470 evaluation board.